CLEAN VERSION OF ALL PENDING CLAIMS

In the Claims:

1. (Amended) A method for forming a spacer, comprising:

depositing a first oxide layer over at least two adjacent polysilicon lines in each of a core area and a periphery area;

performing a first spacer etch in the core area and the periphery area;

implanting an area located between at least two adjacent polysilicon lines in the core area;

applying a second oxide layer over the core area and the periphery area; and

performing a second spacer etch over the periphery area, the core area retaining an amount of the second oxide between the adjacent polysilicon lines while the periphery area is deplete of the second oxide between its adjacent polysilicon lines.

2. (Amended) The method of claim 1 wherein the first oxide layer has a thickness of less than one-half the distance between adjacent polysilicon lines.

3. A non-volatile memory device made by the method of claim1.

4. A non-volatile memory device made by the method of claim 2.

5. (Amended) A process for fabricating a non-volatile memory device comprising:

providing a substrate having a core area, a periphery area, and at least two adjacent polysilicon lines in each of the core area and the periphery area;

depositing a first oxide layer over the adjacent polysilicon lines;

performing a first spacer etch in the core area and the periphery area;

implanting an area located between at least two adjacent polysilicon lines in the core area;

depositing a second oxide layer over the core area and the periphery area; and

performing a second spacer etch over the periphery area.

Cont B3

6. (Amended) The process of claim 5, wherein the first oxide layer has a thickness of less than one-half the distance between adjacent polysilicon lines.

7. The process of claim 5 further comprising performing a second spacer etch over the core area.

8. The process of claim 5, wherein the implanting of an area occurs after the performing of the first spacer etch.

9. The process of claim 5, further comprising implanting an area located between at least two polysilicon lines in the periphery area.

10. The process of claim 9, wherein the implanting of an area located between at least two polysilicon lines in the periphery area occurs after the performing of the first spacer etch.

11. The process of claim 9, wherein the implanting of an area located between at least two polysilicon lines in the core area occurs after the performing of the second spacer etch.

12. A process for making an electronic component comprising:

forming a memory cell by the process of claim 5; and

forming the electronic component comprising the memory cell.

B4

13. (Amended) A process for fabricating a memory cell comprising the steps of:

providing a substrate having a core area, a periphery area, at least two adjacent polysilicon lines in each of the core area and the periphery area, and first spacers adjacent at least two adjacent polysilicon lines in each of the core area and the periphery area; and

forming a second spacer adjacent at least one first spacer.

14. The process of claim 13, further comprising implanting an area located between at least two polysilicon lines in the core area.